REMARKS / ARGUMENTS

Claims 1-13 remain pending in this application. Claims 14-27 have been canceled without prejudice or disclaimer. No new claims have been added.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority and safe receipt of the priority document.

Information Disclosure Statement

Applicants have noticed that in the Information Disclosure Statement filed on April 22, 2004, the publication date listed for JP 2001-156618 was incorrect on the PTO-1449 Form. Therefore, the correct publication date is included in the attached PTO-1449 Form.

35 U.S.C. §112

Claim 1 has been amended to overcome the Examiner's rejection under this section. The Examiner is hereby invited to contact the undersigned by telephone if any further changes are deemed necessary.

35 U.S.C. §§102 and 103

Claims 1-8 stand rejected under 35 U.S.C. §102(e) as being anticipated by Mooney et al (U.S. Patent No. 6,774,287). Claims 1-4 stand rejected under 35 U.S.C. §102(e) as being anticipated by Sine et al (U.S. Patent No. 6,366,867). Claims 9-11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mooney et al. These rejections are traversed as follows.

The present invention is directed to a semiconductor integrated circuit having an output circuit with plural output MOSFETs connected in parallel. These output MOSFETs are divided into plural groups which are respectively divided into plural subgroups. A first control means selects, from the plural output MOSFETs, a number of output MOSFETs to be turned ON to control output impedance and forms selections signals. A second control means controls a slew rate by controlling a drive signal of the output MOSFETs that are turned ON and forms timing signals. Plural output prebuffers are coupled to the output MOSFETs and receive each of the selection signals, timing signals and data signals to be outputted and drive the plural output MOSFETs. The first control means controls output impedance while the second control means controls a slew rate. The first and second control means operate independently.

None of the cited references disclose or suggest these features of the presently claimed invention. Mooney et al disclose a bi-directional communication system having a driver capable of controlling a slew rate of a transmission data

signal. As shown in Fig. 6, driver 300 having legs, 302_0 to 302_n, which include NAND gates 306, 308 which provide a control signal to transistors 307, 309 (see column 4, lines 65-66). The Examiner attempts to equate NAND gates 306, 308 with the predriver of the present invention. However, these NAND gates receive enable signals En0 to En3 and TAP signals TAP0 to TAP3. Enable signals En0 to En3 are used to selectively enable legs (see column 4, lines 49-51) and as such may be more relevant to the selection signal of claim 1. TAP0 to TAP3 are provided from a delay circuit 200 having a plurality of delay stages. By controlling the delay time between each TAP signal, the driver circuit can approximate the ideal slew rate control circuit. An output signal has a plurality of discreet steps in accordance with the number of TAP signals (see column 4, lines 6-21, and Fig. 3).

On the other hand, the present invention neither includes any delay line for slew rate control nor outputs an output signal which has a plurality of discreet steps in accordance with the number of tap signals. As such, it is submitted that the pending claims patentably define the present invention over Mooney et al.

Sine et al disclose a method and apparatus for providing controllable compensation factors to a compensated driver circuit. As shown in Fig. 2, an impedance control circuit 250 is connected in series with a slew control 230. When transistor 232 for slew control is connected in series with transistor 252 for impedance control, slew control and impedance control cannot be performed independently.

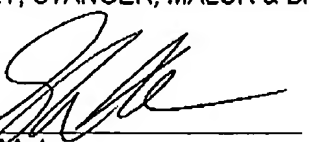
According to the present invention, an output circuit has plural output MOSFETs connected in parallel. From these plural output MOSFETs, the number of output MOSFETs to be turned ON is selected by a first control means to control output impedance. Slew rate is controlled by a second control means controlling a drive signal of the output MOSFETs to be turned ON. Therefore, impedance control and slew rate control are performed independently (see paragraphs [0011], [0012] and [0013] and Fig. 1 of the corresponding publication No. 2004/0251940). As such, it is submitted that the pending claims patentably define the present invention over the cited art.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.



By
Shrinath Malur
Reg. No. 34,663
(703) 684-1120